Use of Nanoparticles and Nanoplatelets in Low-Power Non-volatile Charge Trapping Memory Devices

Ammar Nayfeh and Nazek El-Atab
Institute Center for Microsystems – iMicro, Department of Electrical Engineering and Computer Science (EECS), Masdar Institute of Science and Technology Abu Dhabi, United Arab Emirates

Recently, one of the main developments and application of FLASH memory is flexible, low-cost and reliable solid state memory, such as removable memory, non-volatile memory for portable electronics and solid-state hard drive. For the next-generation electronics, the research of non-volatile memory focus on fast programming/erasing and low-power applications for excellent portable electronics and extremely long battery life [1]. It has been reported that it is possible to reduce the operating voltage of silicon-oxide-nitride-oxide-silicon memory devices from 10 V down to 4 V by reducing the tunnel oxide thickness, however, the retention characteristic of the memory will be reduced from 10 years down to a couple of seconds [2]. Therefore, the investigation of novel materials to be incorporated within current non-volatile memory devices is crucial. In this work, Si and InN nanoparticles, and graphene nanoplatelets are studied as the charge trapping layers of charge trapping memory devices [3-6].

The active layers of the memory devices were deposited using Atomic Layer Deposition, and the nanoparticles were spin coated on the samples. Electrical measurements such as I-V and high-frequency C-V measurements are conducted on the samples in order to study the effect of embedding the nanoparticles/nanoplatelets in the memory cells. The results show that large memory windows can be obtained due to the large charge trapping density of the nanoparticles/nanoplatelets. In addition, the measured retention characteristics are excellent which is due to the large band offset between the nanoparticles and tunnel oxide which exponentially reduce the leakage current. Moreover, using nanoparticles within the charge trapping layer allows for reducing the tunnel oxide thickness without degrading the retention characteristic of the memory.

Furthermore, smaller Si nanoparticles (2-nm average size) showed hole storage while larger nanoparticles (2.85-nm) showed mixed charge storage. This is due to the smaller electron affinity of the smaller nanoparticles which reduces the conduction band offset with the tunnel oxide and therefore may inhibit electron storage. On the other hand, InN and graphene have very large electron affinities and pure electron storage is observed. In fact, the use of nanoparticles with high electron affinity will enable a memory fully programmed and erased using pure electrons instead of mixed charges which would increase the speed of the write and erase speeds of the cells.

Finally, the charge emission mechanism from Si channel to the nanoparticles through the tunnel oxide is studied for the different samples. The memory with 2-nm Si nanoparticles allowed a large memory window at low operating voltages due to Poole-Frenkel hole emission mechanism, while Phonon-Assisted Tunneling and Fowler-Nordheim Tunneling require higher electric fields across the tunnel oxide and therefore higher operating voltages are needed as in the case of the memory cells with InN and graphene nanoplatelets.

[1] B.Yu, "15nm Gate Length Planar CMOS Transistor", IEDM, pp.937-939, 2001.

[2] Y. King, "Thin Dielectric Technology and Memory Devices", Ph.D dissertation, Univ. of California, Berkeley, CA 1999.

[3] Nazek El-Atab, Berk Berkan Turgut, Ali K. Okyay, Munir Nayfeh, and Ammar Nayfeh, "Enhanced non-volatile memory characteristics with Quattro-layer graphene-nanoplatelets vs. 2.85-nm Si-nanoparticles with asymmetric Al2O3/HfO2 tunnel oxide" Nanoscale Res. Lett, vol. 10, no.1, p. 248, 2015.

[4] Nazek El-Atab, Ayse Ozcan, Sabri Alkis, Ali K. Okyay, and Ammar Nayfeh "Low power zinc-oxide based charge trapping memory with embedded silicon nanoparticles via poole-frenkel hole emission," Appl. Phys. Lett. 104, 013112, 2014.